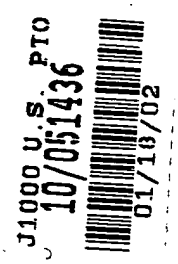
Docket No. END920010051US1



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application: Crossland et al.

Group Art Unit: : IBM Corporation

Examiner: : Intellectual Property Law

Serial No.: : Dept. N50, Bldg. 040-4

Filed: Herewith : 1701 North Street

: Endicott, NY 13760

Title: VIDEO DECODER WITH SCALABLE ARCHITECTURE

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

INFORMATION DISCLOSURE STATEMENT

It is respectfully requested that the publications identified below and listed on the enclosed PTO-1449 Form(s) be considered by the United States Patent and Trademark Office (USPTO) in the subject United States patent application and be made of record therein. A copy of each publication is enclosed, and this submission is otherwise believed to be in compliance with 37 C.F.R. Sections 1.97 and 1.98. This information is all the material information, as defined in 37 C.F.R. Section 1.56(a), of which the submitter is aware. However, no representation is made or intended that a search has been made or that no other such material information exists.

PATENTS

1.	5,576,765	2.	5,742,343	3.	5,929,911
4.	5,963,222	5.	5,973,740	6.	6,055,012
7.	6,057,884	8.	6,128,649	9.	6,157,740

10. "Implementation Of Digital HDTV Video Decoder By Multiple Multimedia Video Processors", C. Lee, et al., IEEE Transactions on Consumer Electronics, Vol. 42, No. 3, August 1996, pps. 395-401.
11. D. Hrusecky, pending U.S. patent application Serial No. 09/237,600, filed January 25, 1999, entitled "Anti-Flicker Logic For MPEG Video Decoder With Integrated Scaling And Display Functions".

None of the above-cited publications, taken singularly or in combination, is believed to teach or suggest the invention as defined by the claims provided in the instant application.

Respectfully submitted,

Dated: October 23, 2001 By: Kevin P. Radigan

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INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
END920010051US1	
Applicant(s)	
Murdock et al.	
Filing Date	**Group Art Unit**
Herewith	

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	AA	5,576,765	11/19/96	Cheney et al.	348	407	
	AB	5,742,343	04/21/98	Haskell et al.	348	415	
	AC	5,929,911	07/27/99	Cheney et al.	348	390	
	AD	5,963,222	10/05/99	Cheney et al.	345	516	
	AE	5,973,740	10/26/99	Hrusecky	348	401	
	AF	6,055,012	04/25/00	Haskell et al.	348	48	
	AG	6,057,884	05/02/00	Chen et al.	348	416	
	AH	6,128,649	10/03/00	Smith et al.	709	217	
	AI	6,157,740	12/02/00	Buerkle et al.	382	233	

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

	AJ	"Implementation Of Digital HDTV Video Decoder By Multiple Multimedia Video Processors", C. Lee, et al., IEEE Transactions on Consumer Electronics, Vol. 42, No. 3, August 1996, pps. 395-401.
	AK	D. Hrusecky, pending U.S. patent application Serial No. 09/237,600, filed January 25, 1999, entitled "Anti-Flicker Logic For MPEG Video Decoder With Integrated Scaling And Display Functions".

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.